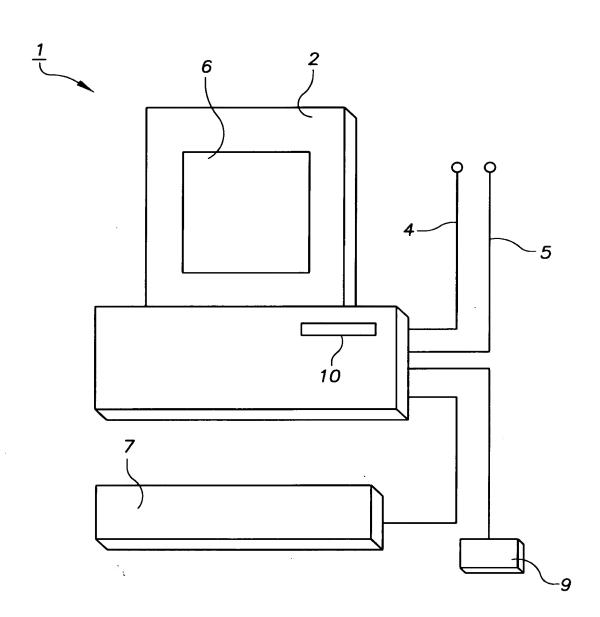
FIG. 1



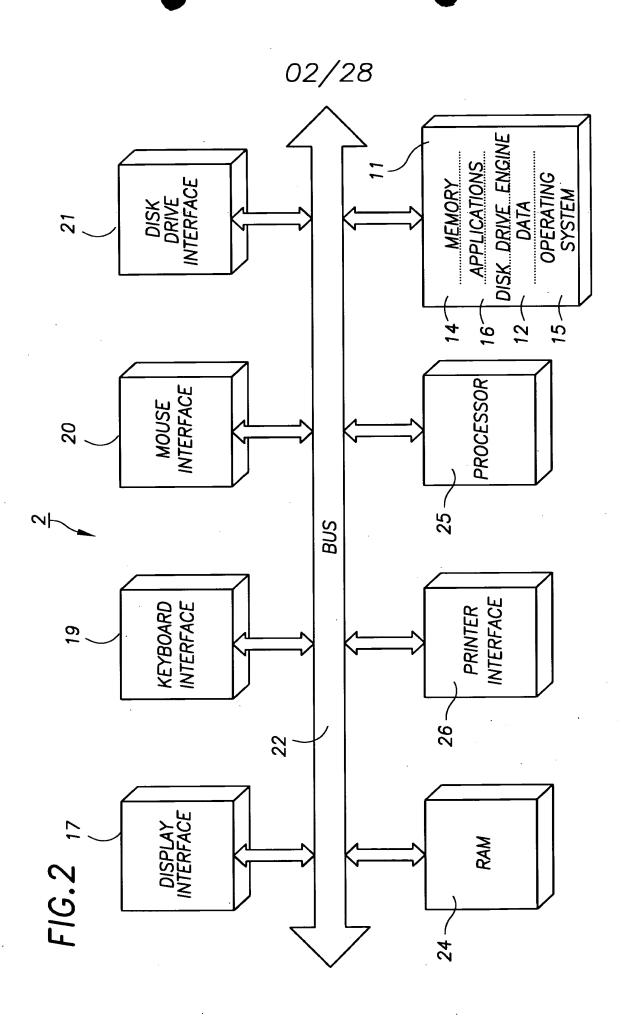
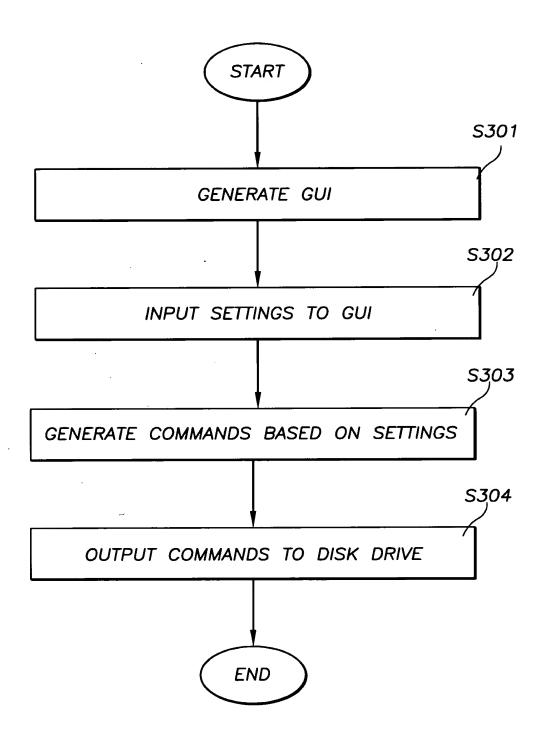


FIG.3



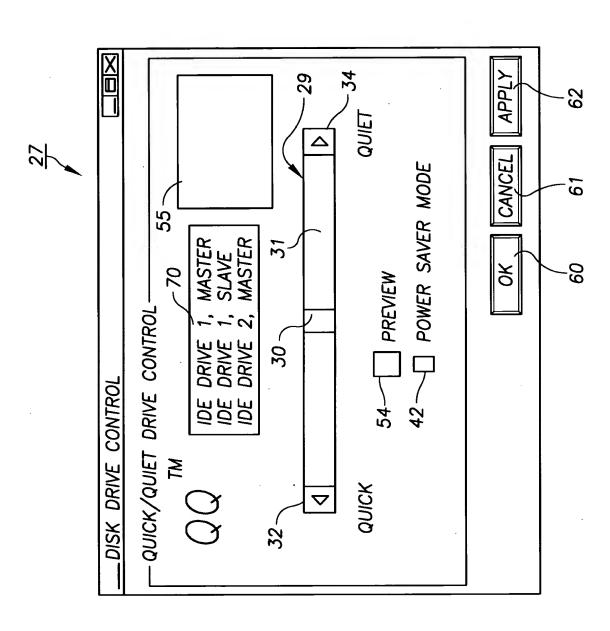
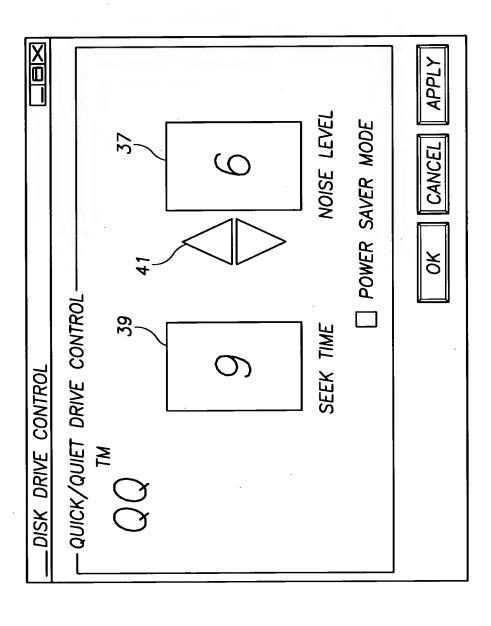
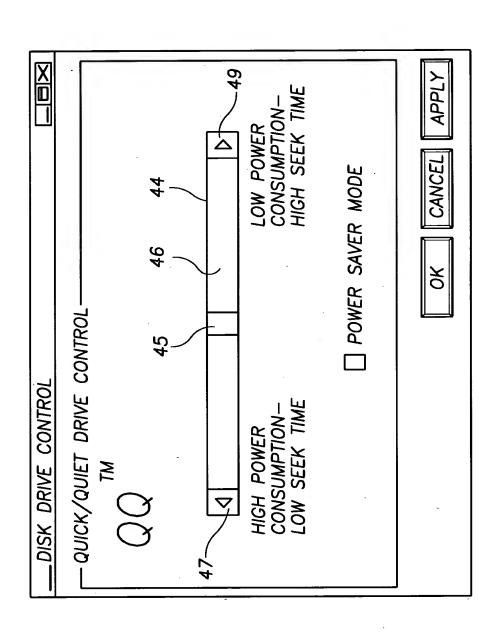


FIG.4



F1G.5



F1G.6

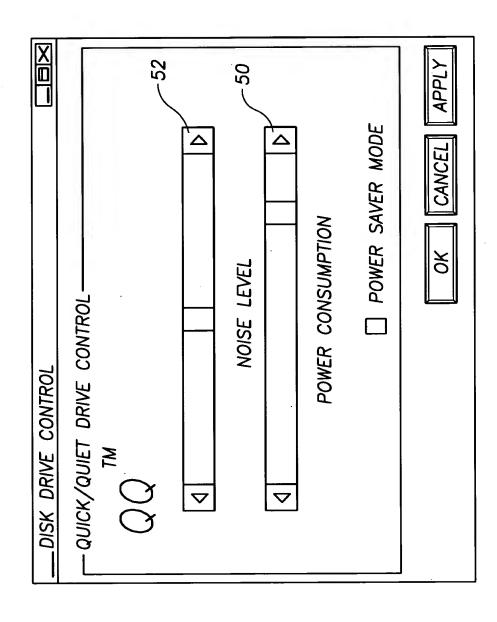
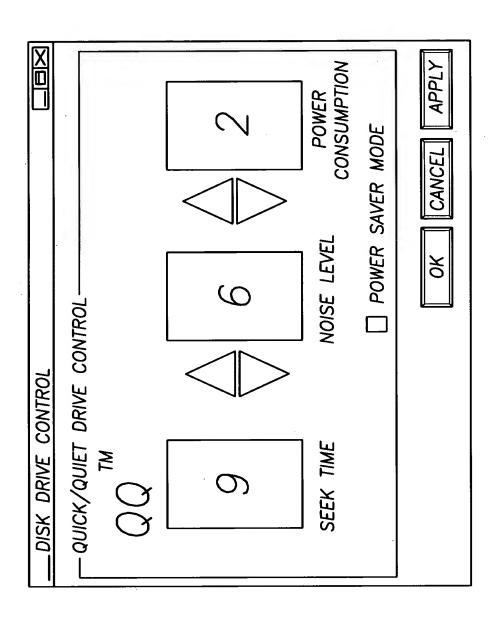


FIG.7



F1G.8

IDE DRIVE 1, MASTER

IDE DRIVE 1, SLAVE

IDE DRIVE 2, MASTER

F1G.9

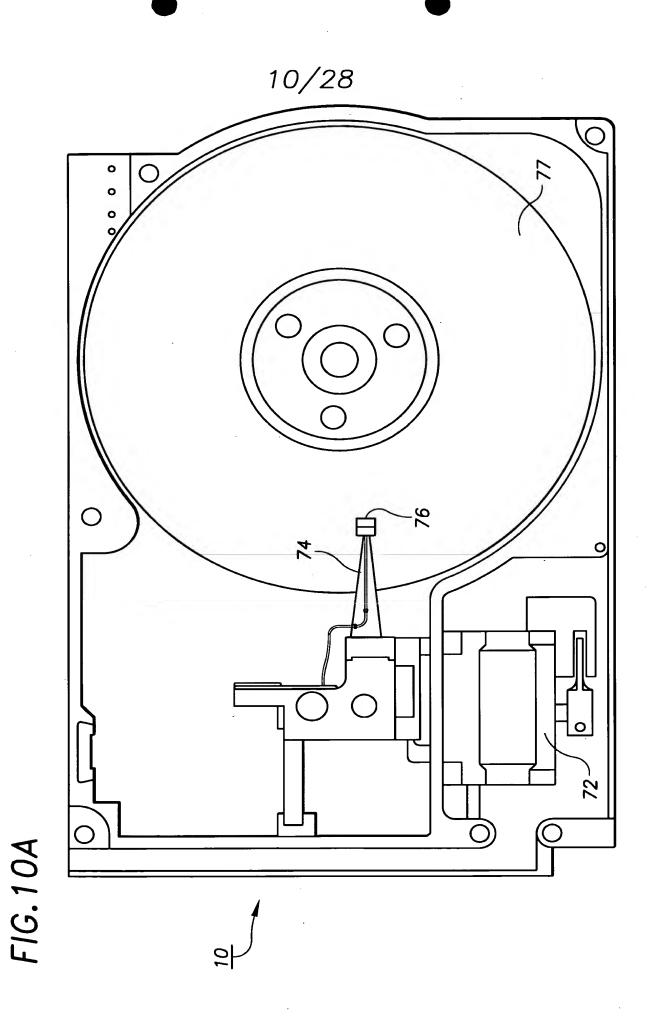
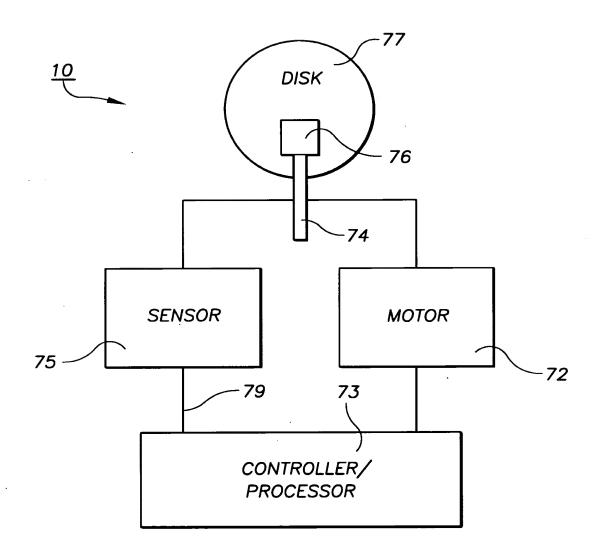


FIG. 10B



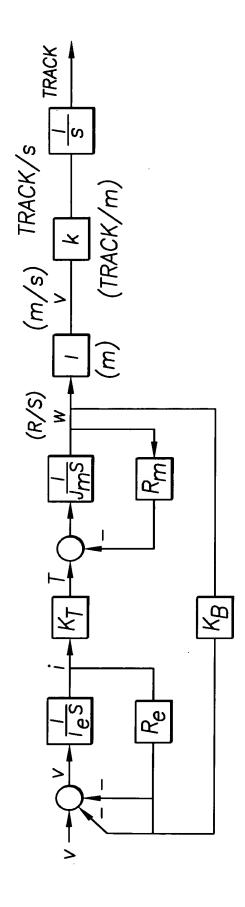
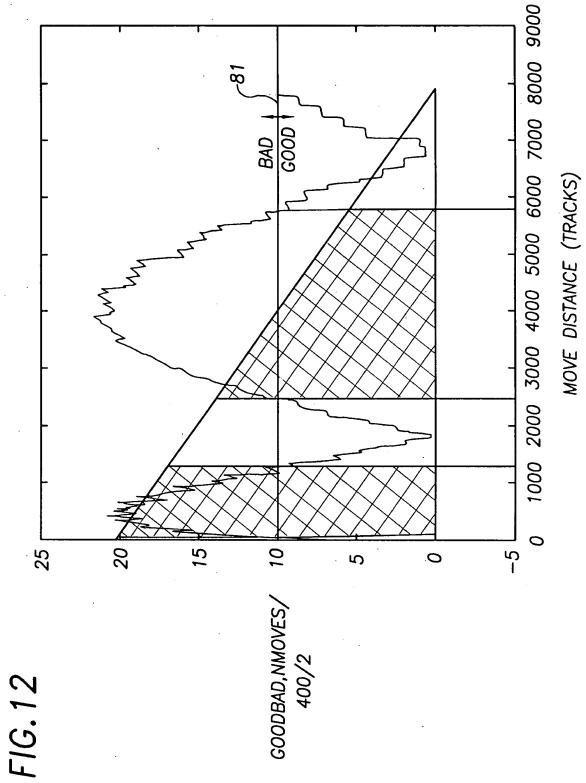


FIG. 11



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FIG. 13
PRIOR ART

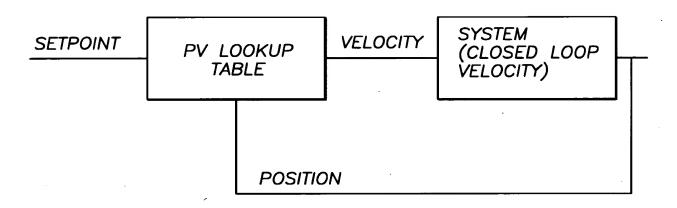


FIG. 14

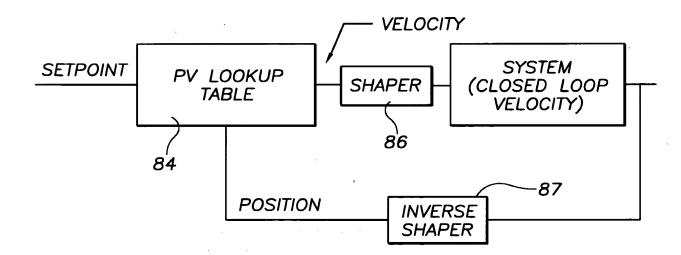


FIG. 15

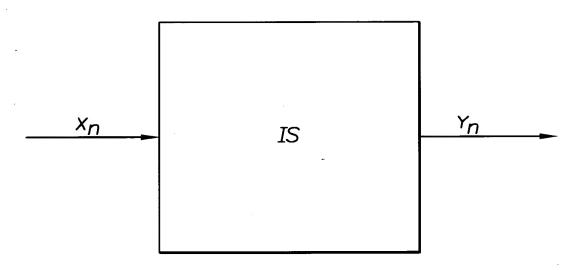


FIG. 16

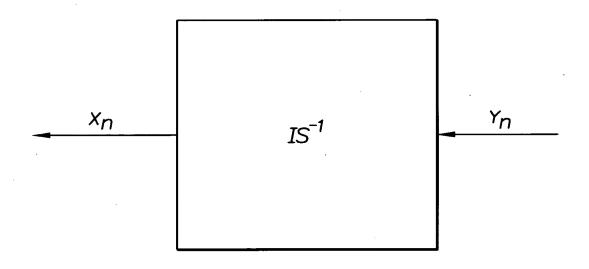


FIG. 17

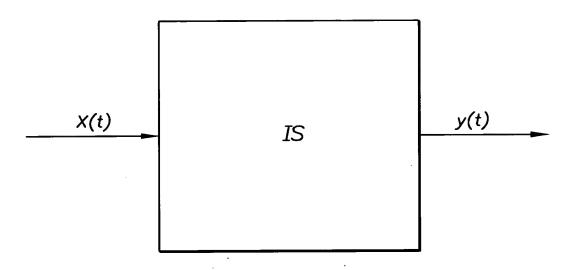


FIG18

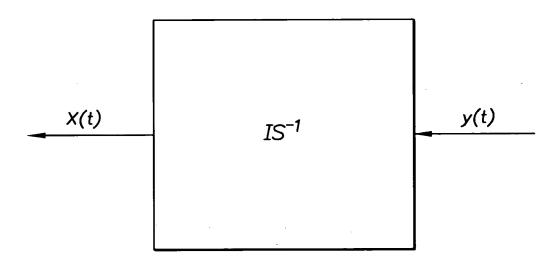


FIG. 19

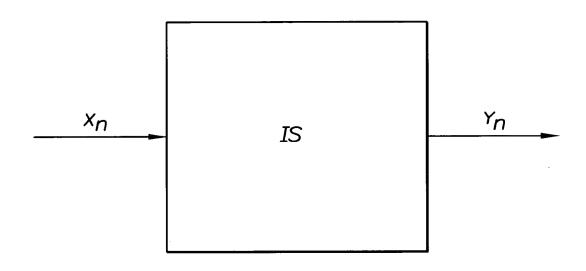
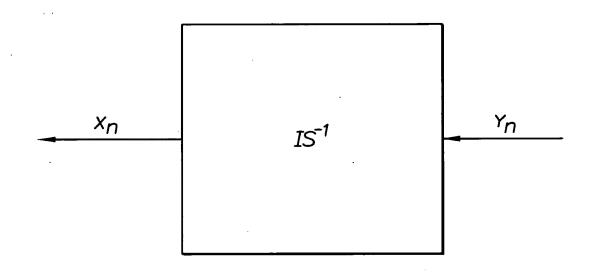


FIG20



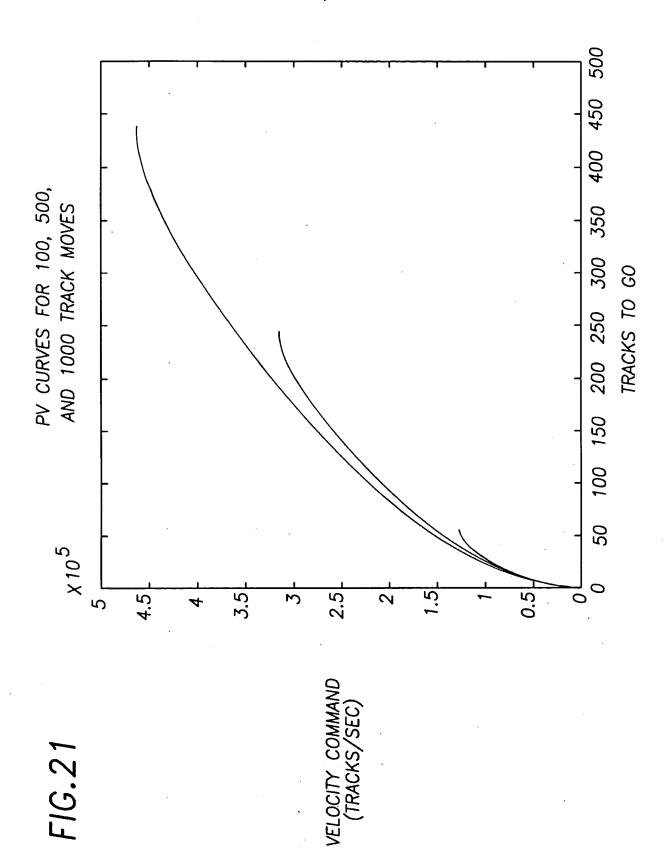
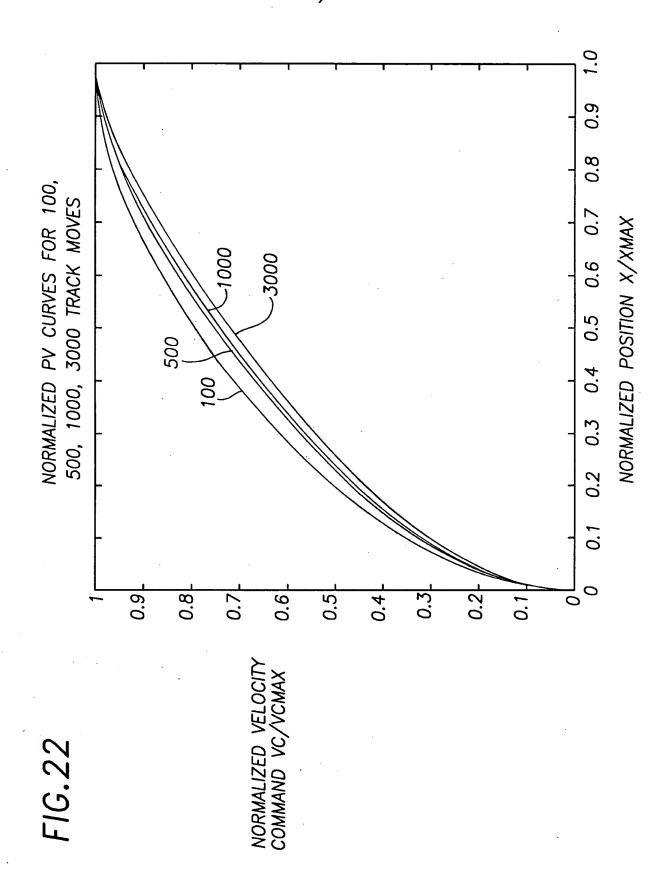
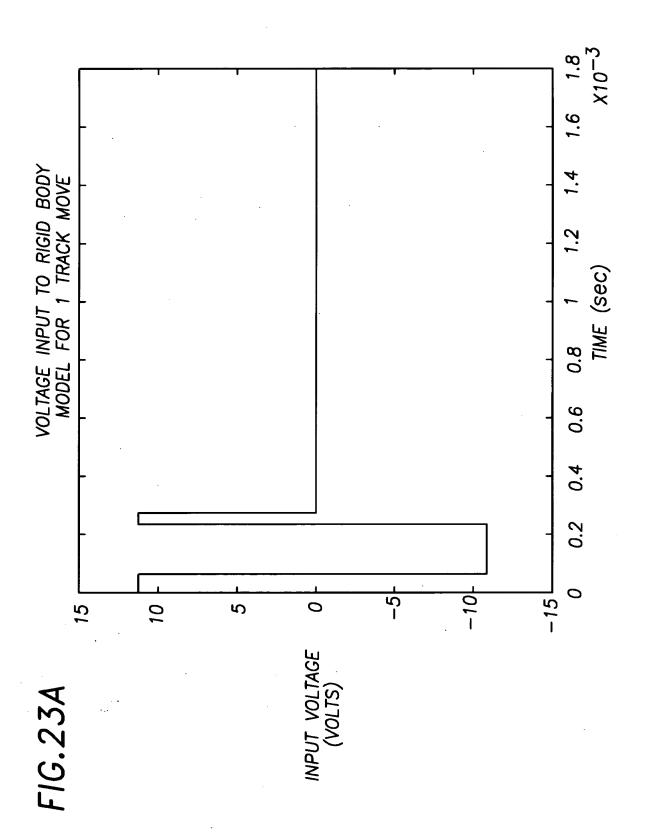
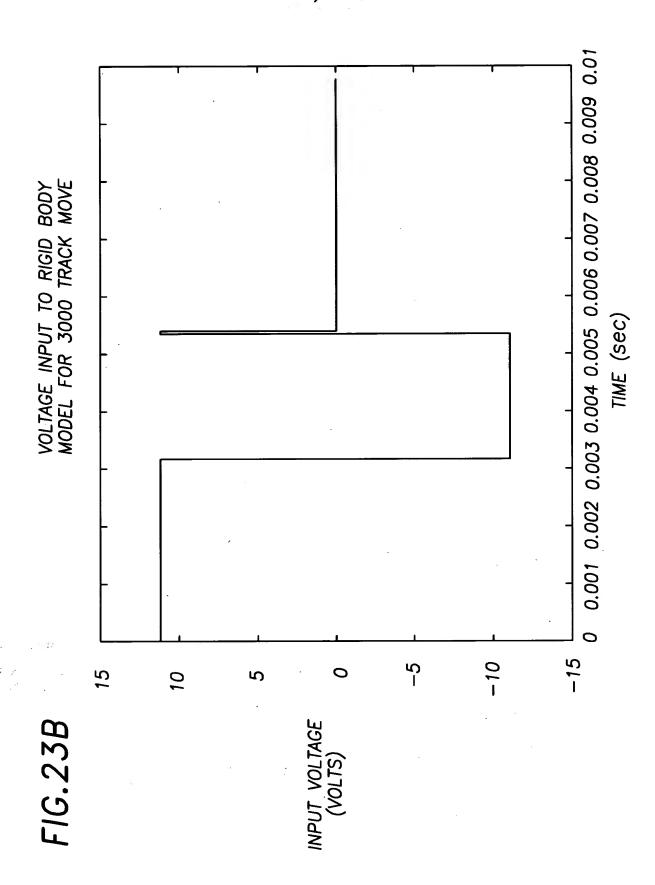


FIG.21







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FIG.24

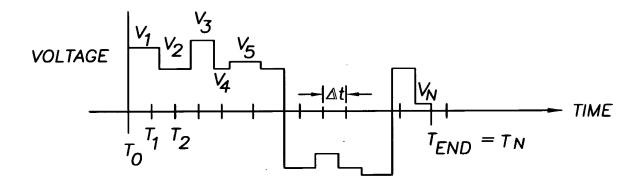


FIG.25

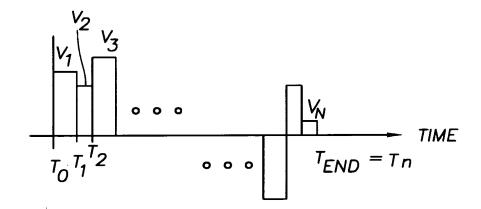


FIG.26

FIG.27

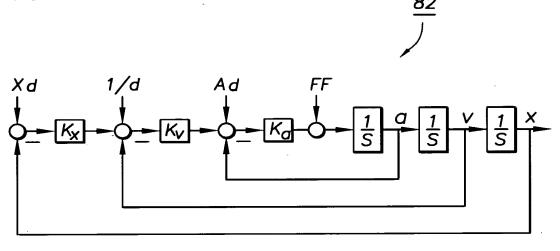
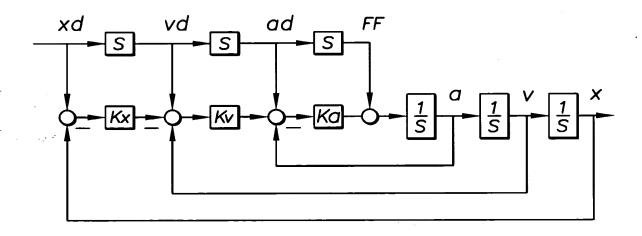
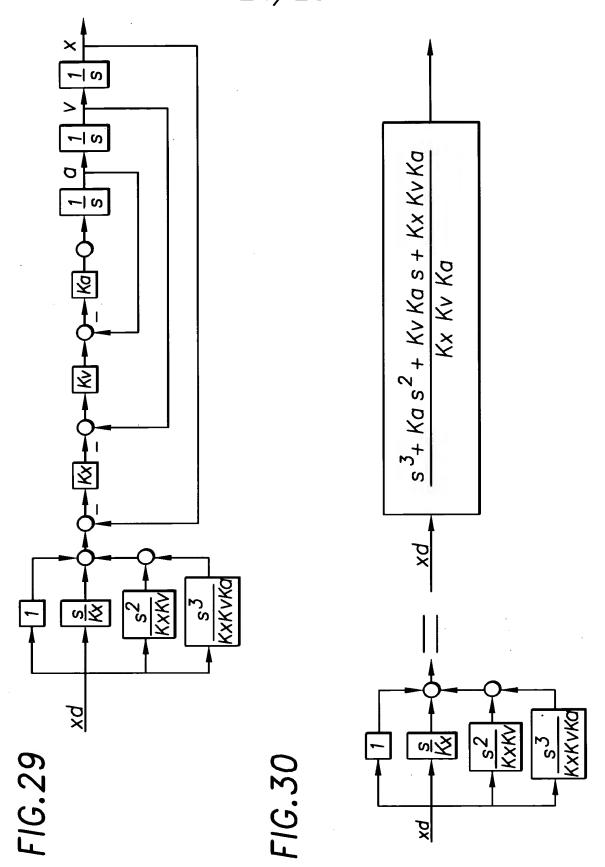
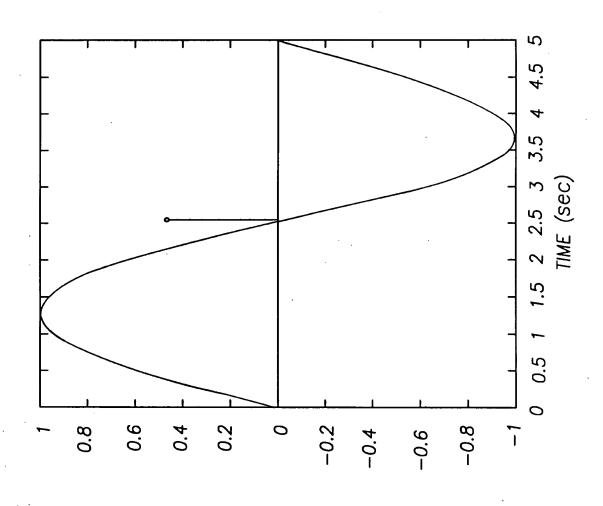


FIG.28





F16.31



AMPLITUDE

FIG.32

FIG.33

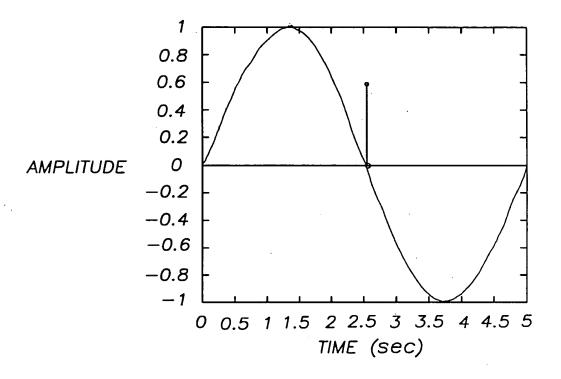


FIG. 34

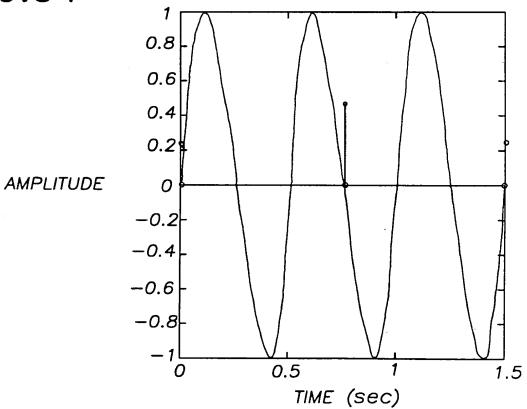


FIG.35

